- **Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})**

- **Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C**

- **Support Unregulated Battery Operation Down to 2.7 V**

- **I_{off} and Power-Up 3-State Support Hot Insertion**

- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**

- **Latch-Up Performance Exceeds 500 mA Per JESD 17**

- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**

SN54LVTH543 . . . JT OR W PACKAGE
SN74LVTH543 . . . DB, DGV, DW, NS, OR PW PACKAGE
(TOP VIEW)

$\overline{LEBA}$	1	24	V_{CC}
$\overline{OEBA}$	2	23	$\overline{CEBA}$
A1	3	22	B1
A2	4	21	B2
A3	5	20	B3
A4	6	19	B4
A5	7	18	B5
A6	8	17	B6
A7	9	16	B7
A8	10	15	B8
$\overline{CEAB}$	11	14	$\overline{LEAB}$
GND	12	13	$\overline{OEAB}$
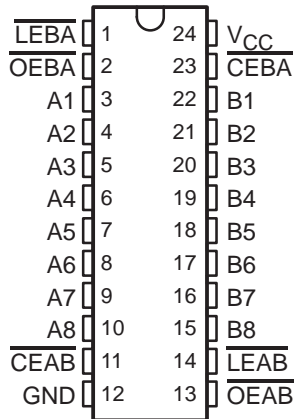
SN54LVTH543 . . . FK PACKAGE
(TOP VIEW)

Top pins: A1, $\overline{OEBA}$, $\overline{LEBA}$, NC, V_{CC}, $\overline{CEBA}$, B1 (4 3 2 1 28 27 26)

Left	Pin	Right	Pin
A2	5	B2	25
A3	6	B3	24
A4	7	B4	23
NC	8	NC	22
A5	9	B5	21
A6	10	B6	20
A7	11	B7	19

Bottom pins: A8, $\overline{CEAB}$, GND, NC, $\overline{OEAB}$, $\overline{LEAB}$, B8 (12 13 14 15 16 17 18)
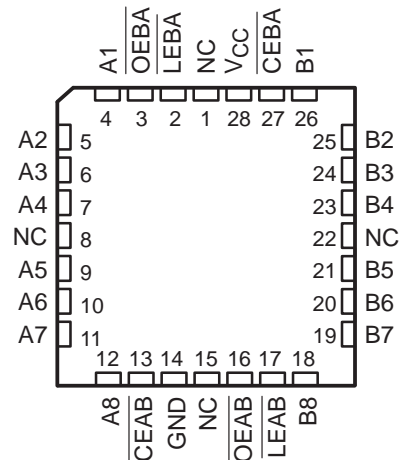
NC – No internal connection

description/ordering information

These octal transceivers are designed specifically for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	SOIC – DW	Tube	SN74LVTH543DW	LVTH543
		Tape and reel	SN74LVTH543DWR	
	SOP – NS	Tape and reel	SN74LVTH543NSR	LVTH543
	SSOP – DB	Tape and reel	SN74LVTH543DBR	LXH543
	TSSOP – PW	Tube	SN74LVTH543PW	LXH543
		Tape and reel	SN74LVTH543PWR	
	TVSOP – DGV	Tape and reel	SN74LVTH543DGVR	LXH543
−55°C to 125°C	CDIP – JT	Tube	SNJ54LVTH543JT	SNJ54LVTH543JT
	CFP – W	Tube	SNJ54LVTH543W	SNJ54LVTH543W
	LCCC – FK	Tube	SNJ54LVTH543FK	SNJ54LVTH543FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

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TEXAS INSTRUMENTS

description/ordering information (continued)

The 'LVTH543 devices contain two sets of D-type latches for temporary storage of data flowing in either direction. Separate latch-enable ($\overline{LEAB}$ or $\overline{LEBA}$) and output-enable ($\overline{OEAB}$ or $\overline{OEBA}$) inputs are provided for each register, to permit independent control in either direction of data flow.

The A-to-B enable ($\overline{CEAB}$) input must be low to enter data from A or to output data from B. If $\overline{CEAB}$ is low and $\overline{LEAB}$ is low, the A-to-B latches are transparent; a subsequent low-to-high transition of $\overline{LEAB}$ puts the A latches in the storage mode. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar, but requires using the $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the device is in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

FUNCTION TABLE[†]

INPUTS				OUTPUT
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0[‡]
L	L	L	L	L
L	L	L	H	H

[†] A-to-B data flow is shown; B-to-A flow control is the same, except that it uses $\overline{CEBA}$, $\overline{LEBA}$, and $\overline{OEBA}$.
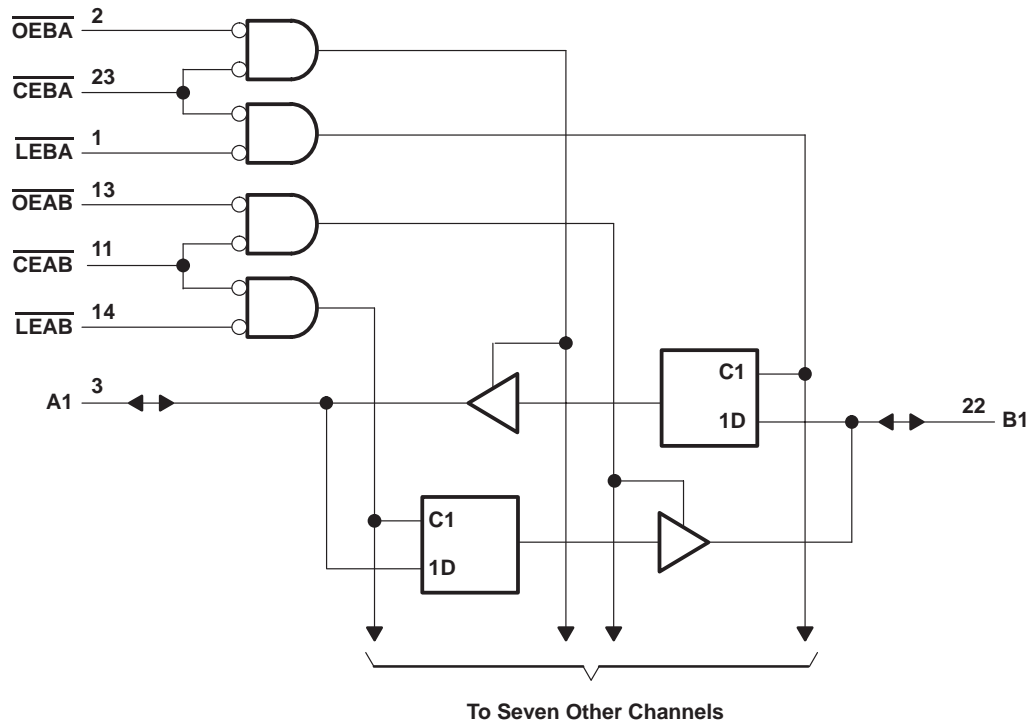
[‡] Output level before the indicated steady-state input conditions were established

logic diagram (positive logic)

To Seven Other Channels

Pin numbers shown are for the DB, DGV, DW, JT, NS, PW, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . −0.5 V to 4.6 V

Input voltage range, V_I (see Note 1) . . . . −0.5 V to 7 V

Voltage range applied to any output in the high-impedance
  or power-off state, V_O (see Note 1) . . . . −0.5 V to 7 V

Voltage range applied to any output in the high state, V_O (see Note 1) . . . . −0.5 V to V_{CC} + 0.5 V

Current into any output in the low state, I_O: SN54LVTH543 . . . . 96 mA
                                                SN74LVTH543 . . . . 128 mA

Current into any output in the high state, I_O (see Note 2): SN54LVTH543 . . . . 48 mA
                                                              SN74LVTH543 . . . . 64 mA

Input clamp current, I_{IK} (V_I < 0) . . . . −50 mA

Output clamp current, I_{OK} (V_O < 0) . . . . −50 mA

Package thermal impedance, θ_{JA} (see Note 3): DB package . . . . 63°C/W
                                                       DGV package . . . . 86°C/W
                                                       DW package . . . . 46°C/W
                                                       NS package . . . . 65°C/W
                                                       PW package . . . . 88°C/W

Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and
   functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not
   implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
        2. This current flows only when the output is in the high state and V_O > V_{CC}.
        3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			SN54LVTH543		SN74LVTH543		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2.7	3.6	2.7	3.6	V
V_{IH}	High-level input voltage		2		2		V
V_{IL}	Low-level input voltage			0.8		0.8	V
V_I	Input voltage			5.5		5.5	V
I_{OH}	High-level output current			−24		−32	mA
I_{OL}	Low-level output current			48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate		200		200		µs/V
T_A	Operating free-air temperature		−55	125	−40	85	°C

NOTE 4:   All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

![Texas Instruments logo]

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH543			SN74LVTH543			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 2.7 V,	I_I = –18 mA			–1.2			–1.2	V
V_{OH}		V_{CC} = 2.7 V to 3.6 V,	I_{OH} = –100 μA	V_{CC}–0.2			V_{CC}–0.2			V
		V_{CC} = 2.7 V,	I_{OH} = –8 mA	2.4			2.4			
		V_{CC} = 3 V	I_{OH} = –24 mA	2						
			I_{OH} = –32 mA				2			
V_{OL}		V_{CC} = 2.7 V	I_{OL} = 100 μA			0.2			0.2	V
			I_{OL} = 24 mA			0.5			0.5	
		V_{CC} = 3 V	I_{OL} = 16 mA			0.4			0.4	
			I_{OL} = 32 mA			0.5			0.5	
			I_{OL} = 48 mA			0.55				
			I_{OL} = 64 mA						0.55	
I_I	Control inputs	V_{CC} = 3.6 V,	V_I = V_{CC} or GND			±1			±1	μA
		V_{CC} = 0 or 3.6 V,	V_I = 5.5 V			10			10	
	A or B ports‡	V_{CC} = 3.6 V	V_I = 5.5 V			20			20	
			V_I = V_{CC}			1			1	
			V_I = 0			–5			–5	
I_{off}		V_{CC} = 0,	V_I or V_O = 0 to 4.5 V						±100	μA
$I_{I(hold)}$	A or B ports	V_{CC} = 3 V	V_I = 0.8 V	75			75			μA
			V_I = 2 V	–75			–75			
		V_{CC} = 3.6 V§	V_I = 0 to 3.6 V						±500	
I_{OZPU}		V_{CC} = 0 to 1.5 V, V_O = 0.5 to 3 V, $\overline{OE}$ = don't care				±100*			±100	μA
I_{OZPD}		V_{CC} = 1.5 V to 0, V_O = 0.5 to 3 V, $\overline{OE}$ = don't care				±100*			±100	μA
I_{CC}		V_{CC} = 3.6 V, I_O = 0, V_I = V_{CC} or GND	Outputs high			0.19			0.19	mA
			Outputs low			5			5	
			Outputs disabled			0.19			0.19	
ΔI_{CC}¶		V_{CC} = 3 V to 3.6 V, One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND				0.2			0.2	mA
C_i		V_I = 3 V or 0				4			4	pF
C_{io}		V_O = 3 V or 0				9			9	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.
‡ Unused terminals are at V_{CC} or GND.
§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

TEXAS INSTRUMENTS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

			SN54LVTH543				SN74LVTH543				UNIT
			V_{CC} = 3.3 V $\pm$ 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$ 0.3 V		V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration,	$\overline{LEAB}$ or $\overline{LEBA}$ low	3.3		3.3		3.3		3.3		ns
t_{su}	Setup time	A or B before $\overline{LEAB}$ or $\overline{LEBA}\uparrow$ Data high	0.4		0.4		0.4		0.4		ns
		A or B before $\overline{LEAB}$ or $\overline{LEBA}\uparrow$ Data low	1		1.5		1		1.5		
		A or B before $\overline{CEAB}$ or $\overline{CEBA}\uparrow$ Data high	0.2		0.2		0.2		0.2		
		A or B before $\overline{CEAB}$ or $\overline{CEBA}\uparrow$ Data low	0.7		1.2		0.7		1.2		
t_h	Hold time	A or B after $\overline{LEAB}$ or $\overline{LEBA}\uparrow$ Data high	1.5		0.6		1.5		0.6		ns
		A or B after $\overline{LEAB}$ or $\overline{LEBA}\uparrow$ Data low	1.3		1.5		1.3		1.5		
		A or B after $\overline{CEAB}$ or $\overline{CEBA}\uparrow$ Data high	1.6		0.5		1.6		0.5		
		A or B after $\overline{CEAB}$ or $\overline{CEBA}\uparrow$ Data low	1.4		1.6		1.4		1.6		

switching characteristics over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH543				SN74LVTH543						UNIT
			V_{CC} = 3.3 V $\pm$ 0.3 V		V_{CC} = 2.7 V		V_{CC} = 3.3 V $\pm$ 0.3 V			V_{CC} = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN	MAX	
t_{PLH}	A or B	B or A	1.2	3.9		4.5	1.3	2.5	3.7		4.3	ns
t_{PHL}			1.2	3.9		4.5	1.3	2.5	3.7		4.3	
t_{PLH}	$\overline{LE}$	A or B	1.2	5.1		6.1	1.3	2.9	4.7		5.9	ns
t_{PHL}			1.2	5.1		6.1	1.3	2.9	4.7		5.9	
t_{PZH}	$\overline{OE}$	A or B	1	5.1		6.4	1.1	2.9	4.9		6.2	ns
t_{PZL}			1	5.1		6.4	1.1	3.2	4.9		6.2	
t_{PHZ}	$\overline{OE}$	A or B	1.9	5.6		6.2	2	3.4	5.3		5.9	ns
t_{PLZ}			1.9	5.6		6.2	2	3.7	5.3		5.9	
t_{PZH}	$\overline{CE}$	A or B	1.2	5.5		7	1.3	3.2	5.3		6.8	ns
t_{PZL}			1.2	5.5		7	1.3	3.5	5.3		6.8	
t_{PHZ}	$\overline{CE}$	A or B	2.2	5.7		6.2	2.3	3.8	5.4		5.9	ns
t_{PLZ}			2.2	5.7		5.9	2.3	3.9	5.4		5.6	

† All typical values are at V_{CC} = 3.3 V, T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION
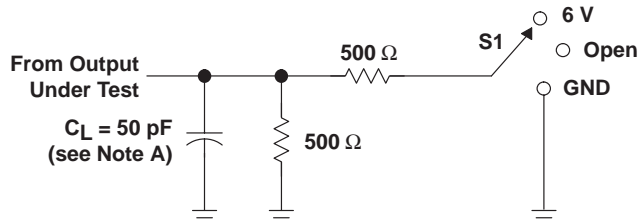
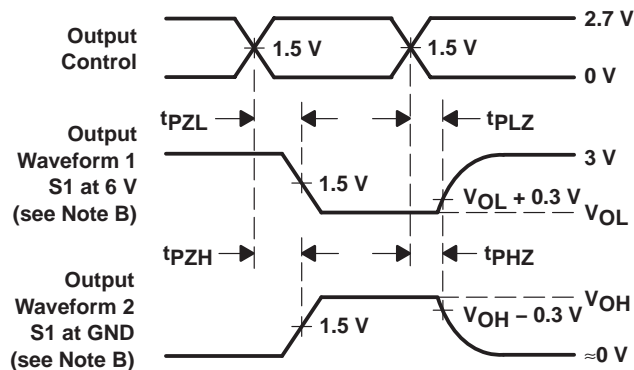| TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	6 V
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT
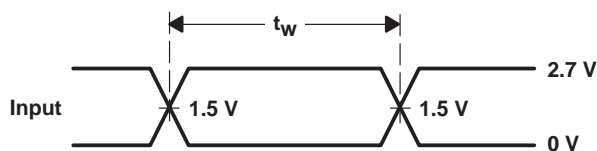
VOLTAGE WAVEFORMS
PULSE DURATION
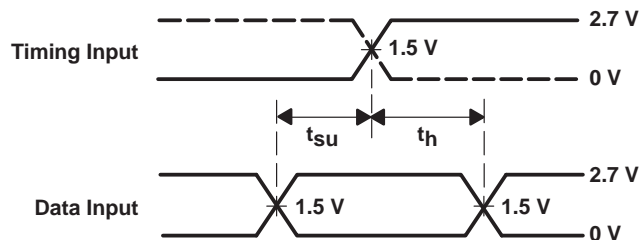
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES
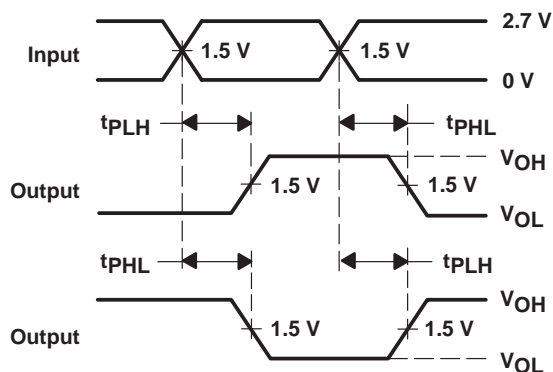
VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
SN74LVTH543DBLE	OBSOLETE	SSOP	DB	24		TBD	Call TI	Call TI
SN74LVTH543DBR	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DBRE4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DBRG4	ACTIVE	SSOP	DB	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DGVR	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DGVRE4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DGVRG4	ACTIVE	TVSOP	DGV	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DWE4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DWG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DWR	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DWRE4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543DWRG4	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543NSR	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543NSRE4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543NSRG4	ACTIVE	SO	NS	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543PWE4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543PWLE	OBSOLETE	TSSOP	PW	24		TBD	Call TI	Call TI
SN74LVTH543PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543PWRE4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVTH543PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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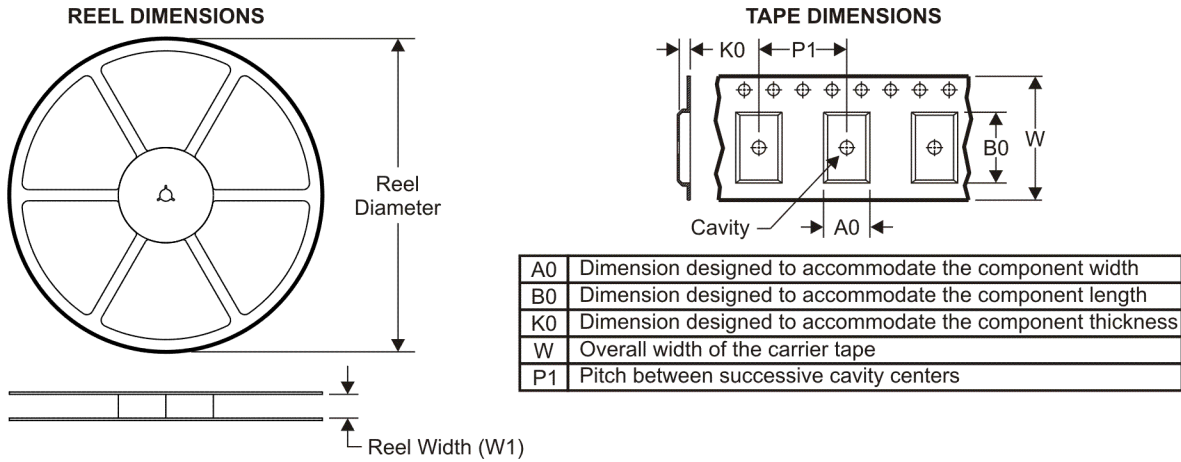
OTHER QUALIFIED VERSIONS OF SN74LVTH543 :
● Enhanced Product: SN74LVTH543-EP

NOTE: Qualified Version Definitions:
    ● Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH543DBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVTH543DGVR	TVSOP	DGV	24	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1
SN74LVTH543DWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVTH543NSR	SO	NS	24	2000	330.0	24.4	8.2	15.4	2.5	12.0	24.0	Q1
SN74LVTH543PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH543DBR	SSOP	DB	24	2000	346.0	346.0	33.0
SN74LVTH543DGVR	TVSOP	DGV	24	2000	346.0	346.0	29.0
SN74LVTH543DWR	SOIC	DW	24	2000	346.0	346.0	41.0
SN74LVTH543NSR	SO	NS	24	2000	346.0	346.0	41.0
SN74LVTH543PWR	TSSOP	PW	24	2000	346.0	346.0	33.0

DB (R-PDSO-G)** PLASTIC SMALL-OUTLINE

28 PINS SHOWN

0,65

$\frac{0,38}{0,22}$ ⊕ 0,15 Ⓜ

28 15

$\frac{5,60}{5,00}$ $\frac{8,20}{7,40}$

$\frac{0,25}{0,09}$

Gage Plane

0,25

0°−8°

$\frac{0,95}{0,55}$

1 14

A

2,00 MAX 0,05 MIN

Seating Plane

⌒ 0,10

DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G)**   **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

	PINS **	14	16	20	24
DIM					
A MAX		10,50	10,50	12,90	15,30
A MIN		9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)**　　　　　　　　　　　　　　　　**PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

0,65

$\dfrac{0,30}{0,19}$　　⊕　0,10 Ⓜ

14　　　8

$\dfrac{4,50}{4,30}$　　$\dfrac{6,60}{6,20}$

1　　7

A

0,15 NOM

Gage Plane

0°−8°

0,25

$\dfrac{0,75}{0,50}$

1,20 MAX　　$\dfrac{0,15}{0,05}$

Seating Plane　　▱ 0,10

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Body dimensions do not include mold flash or protrusion not to exceed 0,15.
　　　　　D.　Falls within JEDEC MO-153

DGV (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE**

24 PINS SHOWN

0,40

$\dfrac{0,23}{0,13}$ ⊕ | 0,07 Ⓜ

24   13

$\dfrac{4,50}{4,30}$ $\dfrac{6,60}{6,20}$

1   12

A

0,16 NOM

Gage Plane

0°−8°

0,25

$\dfrac{0,75}{0,50}$

1,20 MAX

$\dfrac{0,15}{0,05}$

Seating Plane

◁ | 0,08

DIM \ PINS **	14	16	20	24	38	48	56
A MAX	3,70	3,70	5,10	5,10	7,90	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	7,70	9,60	11,20

4073251/E 08/00

NOTES: A. All linear dimensions are in millimeters.
        B. This drawing is subject to change without notice.
        C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
        D. Falls within JEDEC: 24/48 Pins – MO-153
                               14/16/20/56 Pins – MO-194

DW (R−PDSO−G24)   PLASTIC SMALL−OUTLINE PACKAGE

$\frac{0.614\ (15,60)}{0.598\ (15,20)}$

24   13

$\frac{0.419\ (10,63)}{0.393\ (9,97)}$

$\frac{0.299\ (7,60)}{0.291\ (7,40)}$

1   12

Pin 1
Index Area

0.050 (1,27)

$\frac{0.020\ (0,51)}{0.012\ (0,31)}$

⊕ 0.010 (0,25) Ⓜ

0.104 (2,65) Max

$\frac{0.012\ (0,30)}{0.004\ (0,10)}$

$\frac{0.013\ (0,33)}{0.008\ (0,20)}$

△ 0.004 (0,10)

Gauge Plane

Seating Plane

0.010 (0,25)

0°−8°

$\frac{0.050\ (1,27)}{0.016\ (0,40)}$

4040000−5/F 06/2004
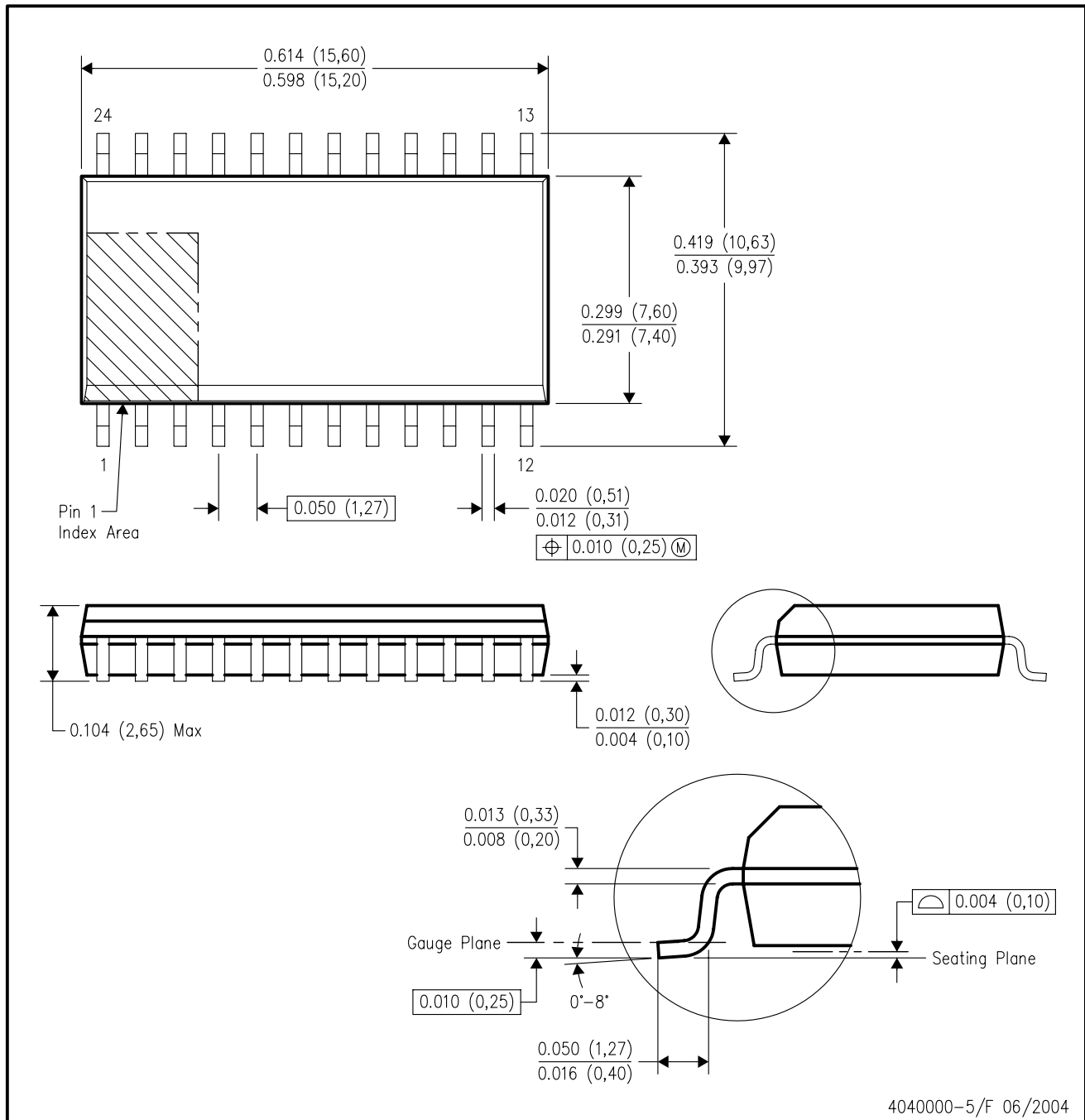
NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS−013 variation AD.

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